WHAT IS CLAIMED IS:

1. A manufacturing method for a wiring circuit substrate, comprising steps of:

preparing a first metal layer used for forming first conductor circuits and selectively forming mask films on one face of said first metal layer;

performing half-etching for said first metal layer by using said mask films as masks, thereby selectively forming protrusions on said one face of said first metal layer;

forming an interlayer-insulating layer on said first metal layer in a state allowing said protrusions to pass through;

overlaying a second metal layer, which will be formed to be second conductor circuits, on said protrusions and said interlayer-insulating layer; and

selectively patterning said first metal layer and said second metal layer at one time or different times, thereby forming said first conductor circuits and said second conductor circuits.

2. A manufacturing method for a wiring circuit substrate according to claim 1, further comprising of step of forming an anisotropic conductive film on top of each of said protrusions before overlaying said second metal layer.

3. A manufacturing method for a wiring circuit substrate according to claim 1, further comprising a step of performing spray-etching for the top of each of said protrusions after forming said protrusions.

4. A manufacturing method for a wiring circuit substrate according to claim 1, wherein said step of forming said protrusions includes a step of using resist masks each having a diameter smaller than a diameter of each said protrusions required to be formed, thereby performing half-etching.

5. A manufacturing method for a wiring circuit substrate according to claim 1, wherein said step of forming said protrusions includes a step of removing the masks after forming said protrusions by performing the half-etching, and a step of performing half-etching again.

6. A manufacturing method for a wiring circuit substrate according to claim 1, further comprising a step of removing unnecessary pieces of said protrusions by performing over-etching before performing patterning for said first conductor circuits and said conductor circuits.